Application of Reverse Bias Recovery Technique to Address PID Issue: Incompleteness of shunt resistance and quantum efficiency recovery

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***Abstract* — Potential Induced Degradation (PID) has recently been identified as one of the major field durability issues of PV modules. The industry is attempting to address this issue at the module/cell production level by modifying the cell, glass and/or encapsulant properties and at the system level through the application of reverse bias voltage during the nighttime. However, there is a lingering question on the full recovery of the cells through the reverse bias application technique. The results obtained in this work indicate that the near-full recovery of efficiency at high irradiance levels can be achieved but the full recovery of efficiency at low irradiance levels, the shunt resistance and the quantum efficiency at low wavelengths could not be achieved.**

***Index Terms* — durability, high voltage, PID, reliability, quantum efficiency, shunt resistance**

I. Introduction

Recent experience in the field indicates that the leakage current between the cell and frame through encapsulant and glass superstrate due to high operating system voltages could cause substantial performance degradation, called potential induced degradation (PID) [1]. It has been observed that PID-stressed modules showed significant output power decrease (~30%) and increase of hot spot risk [1, 2]. In response to this field issue, a new IEC standard for PID is being developed [3]. The performance degradation of negatively grounded systems with p-base Si cells has primarily been attributed to the migration of sodium ions from the glass superstrate to the cell junction [4, 5]. This issue could technically be addressed at the cell/module manufacturing level or at the installed system level. At the manufacturing level, the PID issue can be addressed by modifying the silicon nitride anti-reflection coating, preventing ion conduction through encapsulant or eliminating sodium content in the glass superstrate. If the system is already installed in the field with PID susceptible cells/modules, the PID issue can still be addressed by applying a reverse voltage on the modules during the nighttime [6]. Since the energy consumption during this recovery period is so small as compared to the energy production during the daytime, the reverse bias approach to address the PID issue has been implemented by many system owners. However, it is yet to be demonstrated if the recovery is complete in terms of efficiency at high and low irradiance levels, shunt resistance of cells and the quantum efficiency at all wavelengths. The objective of this paper is to identify the effectiveness of reverse bias on the recovery of the PID subjected cells.

II. Experiments

For this investigation, test coupons (one-cell laminates) were built using common commercial grade construction materials of glass, EVA, cell and backsheet. The experiments were performed using 156mm x 156mm size p-base mono-Si cells, which are susceptible to the PID issue. The PID stress experiments were carried out at −600V for 88 hours at two different temperatures (60°C and 85°C) with 0% relative humidity (RH). Front glass was fully covered with an adhesive conductive aluminum tape to obtain uniform conductivity throughout the glass surface. The negative voltage was applied to the shorted leads of test cell-coupon and the positive voltage was applied on the aluminum tape applied on the front glass as shown in Fig. 1.

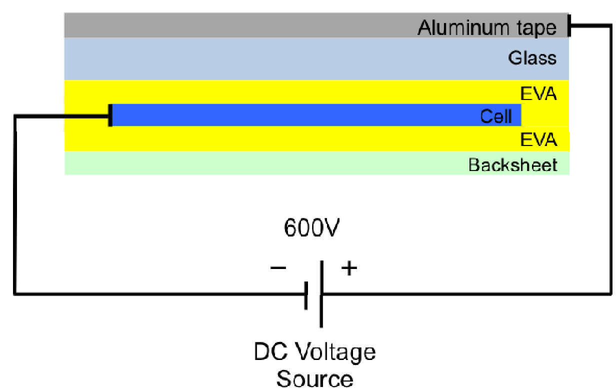

Fig. 1. Schematic of the PID test setup

Before and after the PID test, all test samples were characterized by light I-V (LIV), dark I-V (DIV), electroluminescence imaging (EL), infrared imaging (IR), and quantum efficiency (QE). A steady state solar simulator was used to take the I-V measurements. The recovery experiments were carried out using a reverse bias of +600V for 88 hours at 60°C, 0%RH. Those reverse bias subjected samples were characterized using the techniques identified above and then stored at room temperature without any imposed bias voltage and periodically characterized to observe additional recovery, if any. Also, some of the PID stressed samples that were not subjected to reverse bias recovery were stored and periodically characterized at room temperature to compare the recovery rates between the reverse biased samples and room temperature stored samples. The recovery rate and extent are reported in terms of: Power recovery at both high and low irradiances; Shunt resistance recovery, and; quantum efficiency recovery at all wavelengths between 350 and 1100 nm.

III. Results And Discussion

A. Incomplete Recovery of Power and Shunt Resistance

Fig. 2 shows the progress of PID and recovery of maximum power (P_{max}) at 1000 W/m^2 and on shunt resistance. After 88 hours of PID stress at 60°C, the remaining power was determined to be 70% as compared to the initial, and the shunt resistance dropped close to zero ohms. After the PID test, the sample was stored at room temperature with no bias for more than 75 days, and the power at 1000 W/m^2 is determined to be recovered to about 92%. However, the recovery of shunt resistance is still very low although most of the power at this high irradiance level is recovered.

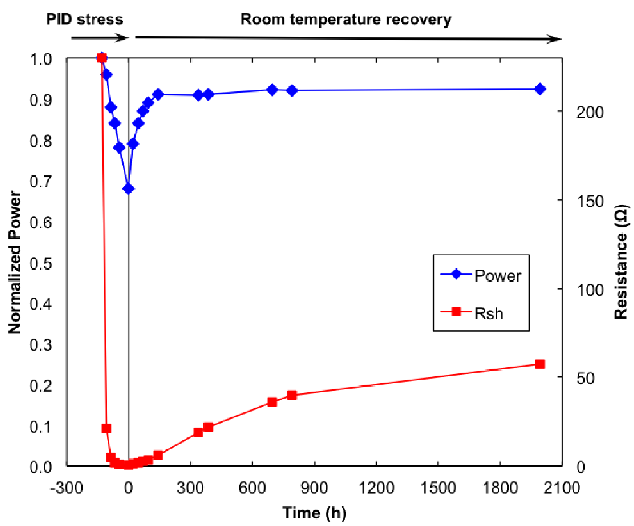

Fig. 2. Recovery rate and level of output power at high (1000 W/m^2) irradiance level, and shunt resistance during the recovery period at room temperature (no aluminum and no bias for 1992h) on a test sample subjected to the PID stress at **60°C/0%RH** (aluminum covered, −600V, 88h).

At 85°C PID stress, much higher power drop in shorter time of test was observed as shown in Fig 3. After leaving at room temperature for more than 500 hours, the recovered power was only 87% at 1000 W/m^2 irradiance level and 60% at 240 W/m^2 irradiance level, and the recovered shunt resistance is practically insignificant. Also, it takes much longer time for both P_{max} and shunt resistance to be recovered as compared to the 60°C-PID stressed samples due to extensive damage to the

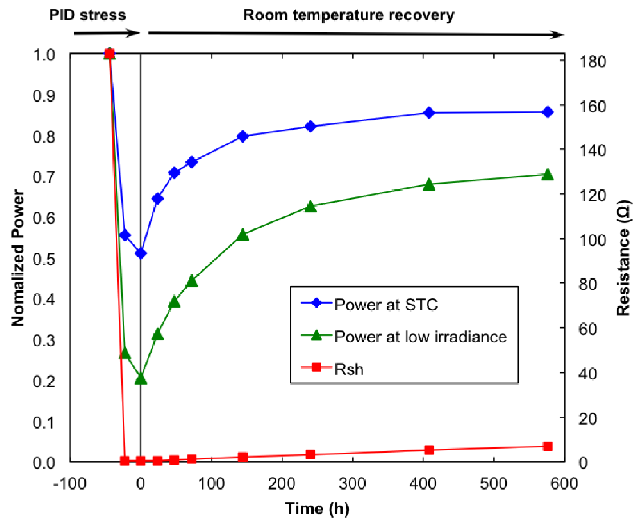

Fig. 3. Recovery rate and level of output power at high (1000 W/m^2) and low (240 W/m^2) irradiance levels, and of shunt resistance during the recovery period at room temperature (no aluminum and no bias for 576h) on a test sample subjected to the PID stress at **85°C/0%RH** (aluminum covered, −600V, 44h).

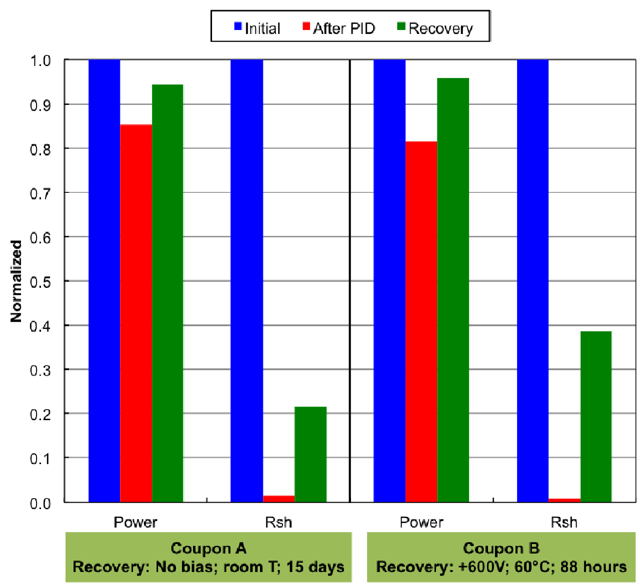

Fig. 4. Normalized power and shunt resistance. Both coupons have the same PID conditions (60°C, −600V, 88h) but different recovery methods. Coupon A: 15-day room temperature storage with no bias, Coupon B: +600V @ 60°C, 88h.

cell materials and/or junction which may not be realistic observation in the field.

In order to observe if an applied reverse voltage at a higher temperature than the room temperature could recover the cells to a higher level, another set of test coupons were prepared and subjected to the tests as shown in Fig. 4. This figure indicates that there is practically no difference, between 0V and +600V bias, in recovery of power at 1000 W/m^2

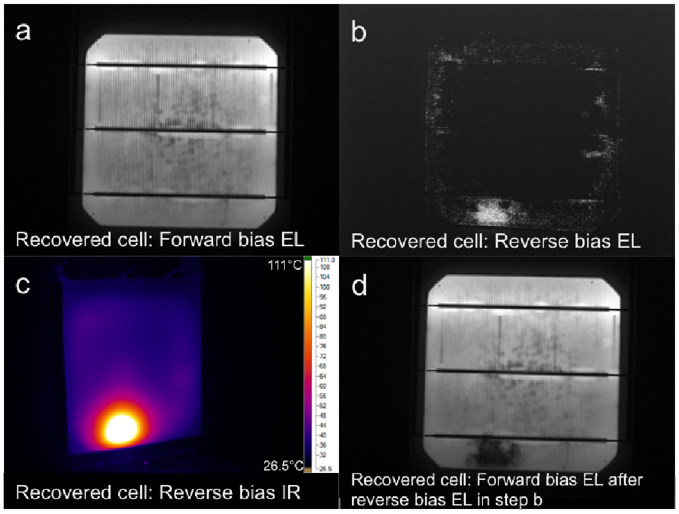

Fig. 5. EL and IR images of 24-day RT stored PID stressed (85°C, 44h) cell. a) Forward bias EL, b) Reverse bias EL, c) Reversed biased IR image, d) Forward bias EL after cell damaged by reverse bias in step b.

irradiance level but there is a significant increase (nearly two times) in shunt resistance due to the voltage bias at +600V. Even though the recovery of power at high irradiance of 1000 W/m^2 is as high as 93% of its original, the recovery of the shunt resistance is still only about 40% of its original. Neither of those cells showed higher than 50% shunt resistance recovery after 125 days room temperature storage. And, recovery speed for both power and shunt resistance is extremely slow after 40-day storage. This poor recovery of shunt resistance would have a serious impact on the cell efficiency at low irradiance levels.

This inadequate shunt resistance recovery could cause: (i) a safety issue if the cells in a module were to operate under shaded/reverse bias condition with failed bypass diodes; (ii) very low energy production at the sites where the module performance primarily depends on the prevailing low light conditions. All the fresh test coupons showed practically 0A current flowing through the cell at −12V. Due to cell shunting after the PID stress, the observed reverse current at −9V was higher than 8A just after the stress test and even after a 24-day recovery period at room temperature. Because of this localized high current, as shown in Fig. 5, the cell was found to be damaged due to high localized temperature. Interestingly, it was observed that this cell was not permanently damaged. The damaged cell was stored at room temperature for 32 days and then I-V and EL were carried out. The results, as shown in Fig. 6, show that there was increase of P_{max} and shunt resistance as compared to the day that cell was damaged due to reverse bias EL measurement. EL images (not shown here) also showed brighter damaged area than before. The cell has been monitored more than 200 days to see if there is complete recovery from PID; however, there has no complete recovery obtained. This result supports that the remained sodium ions in the stacking faults or other regions of the cell are still making a critical impact on PID stressed cells. It is assumed that those remained sodium ions hinder the 100% recovery of shunt resistance and cause very high possibility that PID stressed cells could be easily damaged under reverse bias condition.

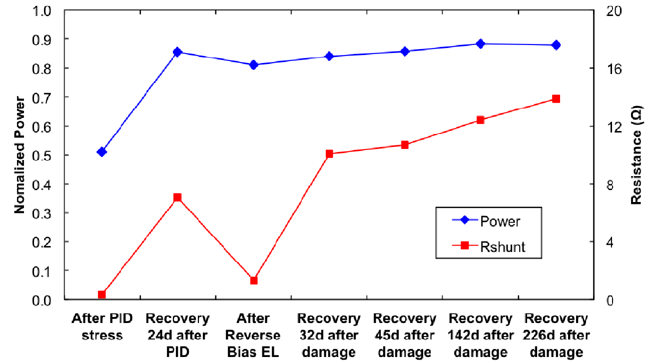

Fig. 6. The recovery method applied for these results is the room temperature storage with no voltage application. The reverse bias imposed during EL decreased the shunt resistance. Initial R_{sh} was 183Ω.

TABLE I

KEY I-V PARAMETERS DURING PID AND RECOVERY

	P_{max} (W)	FF (%)	R_{sh} (Ω)	Current at -12V (A)	Current at -9V (A)	Current at -7V (A)
Initial	3.84	68.0	230	0	0	0
PID stress for 132 h	2.63	50.2	0.59			
Relative to Initial (%)	**-31.53**	**-26.18**	**-99.75**	**NA**	**NA**	**NA**
83-day (1992h) Room temperature storage after PID test	3.55	66.3	57.4		-1.5	-0.4
Relative to Initial (%)	**-7.68**	**-2.50**	**-75.04**	**NA**	**NA**	**NA**

As shown in Table I, even the coupon with 92% power recovery (after 83 days at room temperature) showed a reverse current of 0.4A at −7V and this localized current could be high enough in damaging the cell under reverse bias condition. To further investigate PID effect in terms of light I-V in negative voltage, another coupon was built and PID stressed at 60°C/−600V/88h. Fig. 7 shows I-V curves of the coupon at 240W/m^2 irradiance level, which is a worse performance condition for shunted cell. There was a large reverse current after 88h PID while a fresh cell had no reverse current at all as shown in Fig. 7. The 98h PID recovery of the cell (94% P_{max} at 1000 W/m^2 and 75% P_{max} at low irradiance, respectively) still showed high reverse current due to very slow recovery of R_{sh}. Therefore, it is suggested that R_{sh} should be monitored with P_{max} in evaluating PID recovery. Additionally, it was observed that the increase of reverse current is nonlinear, which supports that shunting caused by PID is not a simple shunting. The presence of localized shunts even after extensive recovery with or without voltage bias indicates the presence of traces of sodium at the junction.

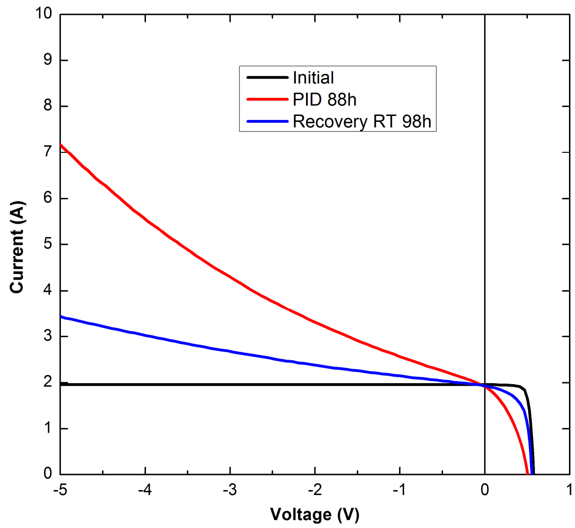

Fig. 7. I-V characteristics of PID stressed and recovered cell at low irradiance (240 W/m^2) (PID 60°C/−600V/88h; PID recovery at room temperature/no bias/98h)

B. Incomplete Recovery of Quantum Efficiency

Fig. 8 shows QE curves of test cell after PID (P_{max}: 81%) and recovery (P_{max}: 96%) steps. As expected, the QE of after-88h-recovery stressed/shunted sample was found to be much lower than the initial; however, the short-circuit current (I_{sc}) obtained after integrating the QE curve and the I_{sc} measured using a white light based I-V tester were found to be not matching. The primary reason for the lower integrated I_{sc} in the QE system as compared to the actual measured I_{sc} is due to the absence of zero (or near zero) impedance in the QE measurement system. Very small impedance in the QE system would not be an issue for the normal high shunt resistance cells but it would be an accuracy issue for the low shunt resistance cells such as PID subjected/recovered cells. This accuracy issue is discussed in another paper presented in this conference [7].

In order to observe if the relative QE curves between the fresh/initial and recovered cell are the identical, these curves were normalized. As shown in Fig. 8, the QE values for the photons between 350 and 500nm wavelength are found to be lower than the QE of fresh/initial cell. This phenomenon was clearer in 85°C PID stressed cell as shown in Fig. 9. None of the QE curves in recovery process were identical to initial at wavelength range from 350-600nm. The penetration depth of these photons on the solar cell [8] is on the order of the junction depth from the surface of the cell, and this indicates that the QE loss in this wavelength range is arising mostly due to the junction shunting caused by the unrecovered sodium in the junction during the reverse bias process. The mechanism for only partial recovery of sodium is not fully understood and it will be a subject of future research.

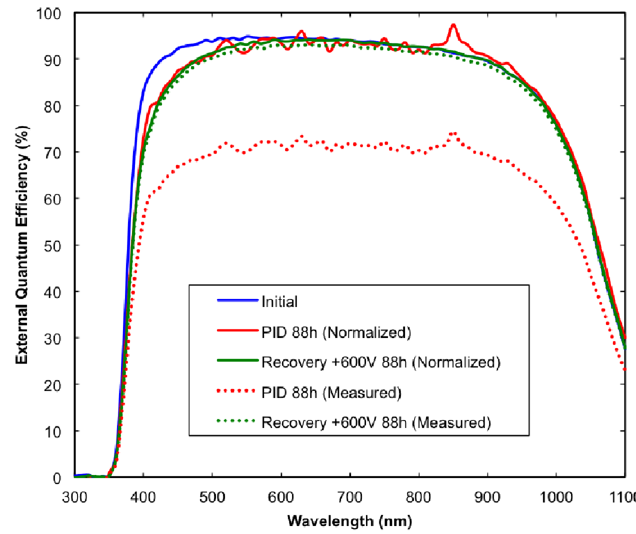

Fig. 8. EQE of fresh/initial, PID stressed and recovered cells (PID stress at 60°C/−600V/88h; PID recovery at 60°C/+600V/88h)

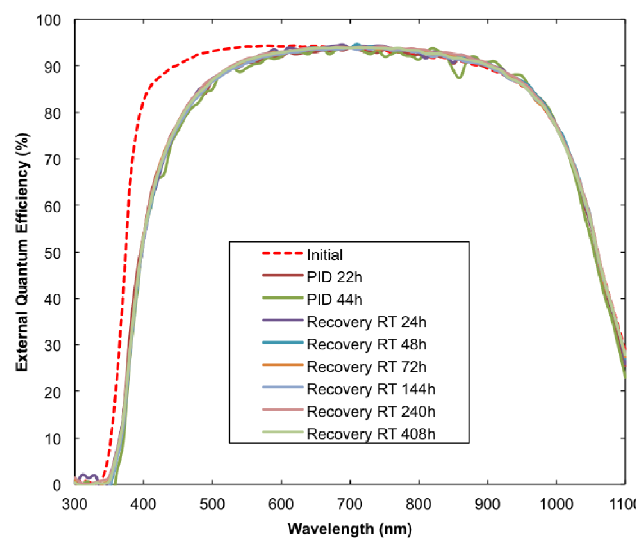

Fig. 9. EQE of fresh/initial, PID stressed and recovered cells (PID stress at 85°C/-600V/44h; PID recovery at RT/no bias/408h) All EQE points are normalized to the initial EQE

Conclusion

The PID recovery methods presented in this paper show very good regeneration (up to 96%) of P_{max} at high irradiance level of 1000 W/m^2. However, the recovery of shunt resistance and efficiency at low irradiance levels is extremely low as compared to the recovery of P_{max}/efficiency at a high irradiance level. The poor cell efficiency at low irradiance levels would lead to lower energy production at predominantly low irradiance level locations and durations. The near-full P_{max} recovered cells still show much higher reverse bias current as compared to the fresh cells. Therefore, any recovered cells/modules through the application of opposite bias and/or high temperature may pose safety risks under shaded condition if the protecting bypass diodes happen to fail in the field. Consequently, just the P_{max} recovery at high irradiance level alone should not be considered as the sole parameter indicating the full recovery from the PID issue as the cells still retain some of the defects caused by the PID damage.

None of the characterization results obtained with I-V (dark and light), EL, and QE showed a complete recovery after the recovery bias or temperature application. Further research is underway to determine the mechanisms/reasons causing only the partial recovery of sodium from the junction.

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