A Droop Controller is intrinsically a Phase-Locked Loop

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***Abstract*—This paper demonstrates that a droop controller, which is fundamental to the operation of power systems and now the parallel operation of inverters, is intrinsically the same as a phase-locked loop (PLL), which is widely adopted in modern electrical engineering. This bridges the gap between the two communities working on droop control and PLLs. As a result, droop controllers and PLLs can be improved and further developed via adopting the advancements in the other community. This also offers insightful understanding to power systems that have inverters and generators mixed together and leads to significant technological breakthrough for the grid connection of renewable energy. For example, there is no longer a need for grid-connected inverters to have a phase-locked loop and a droop controller at the same time.**

I. Introduction

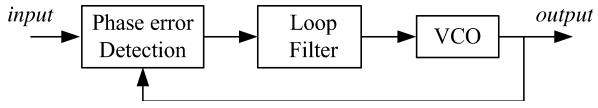
In order to address the energy and sustainability issues being faced worldwide nowadays, more and more renewable energy sources are being connected to power systems, often via DC/AC converters (also called inverters). These inverters are required to synchronise with the system connected to. Another important requirement for these inverters is that they should take part in the regulation of system frequency and voltage, in particular, when the penetration of renewable energy exceeds a certain level.

There are many ways to synchronise an inverter with the grid but the most commonly adopted strategies are based on phase-locked loops [1], [2], [3], of which some examples can be found in the grid connection of renewable energy [4], [5], FACTS devices [6], [7], active power filters [8], UPS applications [9] and power quality control [10]. Phase-locked loops are also widely adopted in other areas of modern electrical engineering, e.g. communication and signal processing. A recent search from ieeexplore.ieee.org with "phase-locked loop" has found more than 5600 papers.

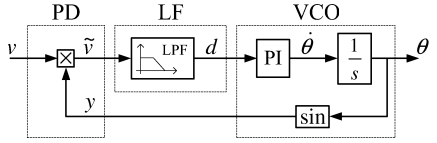
What is fundamental to the operation and regulation of the frequency and voltage of a power system is the so-called droop control strategy. It was originally adopted to operate synchronous generators and have recently been adopted to operate inverters connected in parallel. The generators and/or inverters change the reactive power and real power output according to the system voltage and frequency. A recent search from ieeexplore.ieee.org with "droop control" has found more than 700 papers.

To the best knowledge of the authors, no links between these two strategies have been reported in the literature. In this paper, it is shown that these two strategies are intrinsically the same, which bridges the gap between the two communities.

The rest of the paper is organised as follows. The PLLs and droop control are briefly reviewed in Sections II and III, respectively, and their link is established in Section IV. Conclusions and discussions are made in Section V.



(a) Operational concept



(b) A simple PLL

Figure 1. Block diagrams of a conventional PLL

II. Brief Review of Phase-Locked Loops (PLL)

A. Basic PLL

A basic phase-locked loop (PLL) adopts a control loop to track the phase of an input signal. It can often provide the frequency information of the signal as well, but normally without the information of the voltage amplitude.

The operational principle of a PLL is shown in Figure 1(a). It consists of a phase detection (PD) unit, a loop filter (LF) and a voltage-controlled oscillator (VCO). The PD unit generates a non-zero DC component, often polluted with ripples, when the phase difference between the input signal and the re-produced output signal is not the same. The DC component is extracted and amplified by the LF before being passed to the VCO, which is often a PI controller, to generate the frequency for the output signal. In the steady state, the input to the PI controller is forced to be zero so the phase difference between the input signal and the output signal is zero. As a result, the phase of the output signal is locked with that of the input signal.

Figure 1(b) shows the detailed structure of a basic PLL, where the PD unit is a multiplier, the LF is a low-pass filter (LPF) and the VCO consists of a PI controller, an integrator and a sinusoidal function generator. For an input signal $v = V_m \cos\theta_g$ with phase $\theta_g = \omega_g t + \phi_g$ and an output signal

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$y = \sin\theta$ with phase $\theta = \omega t + \phi$, the output of the PD unit is

$$\begin{aligned}\widetilde{v} = vy &= V_m \sin\theta\cos\theta_g \\ &= \frac{V_m}{2}\sin(\theta-\theta_g) + \frac{V_m}{2}\sin(\theta+\theta_g). \quad (1)\end{aligned}$$

The first term is a low-frequency component that contains the phase difference between v and y and the second term is a high-frequency component, which can be filtered out by the low-pass loop filter. The output $d = \frac{V_m}{2}\sin[(\omega-\omega_g)t + (\phi-\phi_g)]$ of the LF is then fed into a PI controller to generate the estimated frequency $\omega = \dot{\theta}$ until $d = 0$. In the steady state, d is driven to zero and $\theta = \theta_g$, i.e. $\omega = \omega_g$ and $\phi = \phi_g$. The phase of the output signal y is locked with that of the input signal v.

B. Enhanced PLL (EPLL)

Although the basic PLL is able to lock the phase very quickly but no amplitude information about the input signal is available. In order also to obtain the amplitude information of the input signal, an enhanced PLL (EPLL) [11], [12] can be adopted. This method was introduced with several different names, e.g. the sinusoidal tracking algorithm (STA) [13], the amplitude phase model (APM) and amplitude phase frequency model (APFM) [14]. It is able to extract the fundamental component of a periodic signal and, at the same time, to estimate its amplitude, phase and frequency.

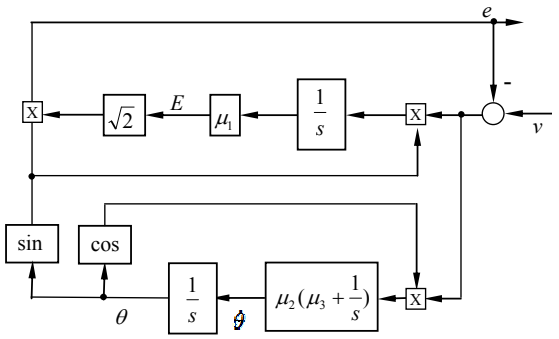


Figure 2. The enhanced phase-locked loop (EPLL) or the sinusoidal tracking algorithm (STA)

The enhanced PLL can be designed by using the gradient descent method [15]. Assume that a typical periodic voltage $v(t)$ has the general form of

$$v(t) = \sum_{i=0}^{\infty}\sqrt{2}V_i\sin\theta_{gi} + n(t)$$

where V_i and $\theta_{gi} = \omega_{gi}t + \delta$ are the RMS value and phase of the i-th harmonic component of the voltage, and $n(t)$ represents the noise on the signal. The objective of a PLL can be regarded as extracting the component $e(t)$ of interest, which is usually the fundamental component, from the input signal $v(t)$. Denote the estimated or recovered signal $e(t)$ as

$$e(t) = \sqrt{2}E(t)\sin(\int_0^t \omega(\tau)\,\mathrm{d}\tau + \delta(t)),$$

where $E(t)$ is the estimated RMS voltage, $\omega(t)$ is the estimated frequency and $\theta(t) = \int_0^t \omega(\tau)\,\mathrm{d}\tau + \delta(t)$ is the estimated phase of $e(t)$. Then the problem of designing a PLL can be formulated as finding the optimal vector $\psi(t) = \begin{bmatrix} E(t) & \omega(t) & \delta(t)\end{bmatrix}^T$ that minimises the cost function

$$J(\psi(t), t) = \frac{1}{2}d^2(t) = \frac{1}{2}[v(t) - e(t)]^2,$$

where $d(t) = v(t) - e(t)$ is the tracking error. According to the gradient descent method [15], this optimisation problem can be solved via formulating

$$\frac{\mathrm{d}\psi(t)}{\mathrm{d}t} = -\mu\frac{\partial J(\psi(t), t)}{\partial\psi(t)}$$

where μ is the diagonal matrix $diag\{\frac{1}{2}\mu_1, \frac{1}{2}\mu_2, \mu_3\}$ chosen to minimise J along the direction of $-\frac{\partial J(\psi(t),t)}{\partial\psi(t)}$. The resulting set of differential equations can be found as [13], [14]

$$\begin{cases} \frac{\mathrm{d}E(t)}{\mathrm{d}t} = \mu_1 d\sin\theta, \\ \frac{\mathrm{d}\omega(t)}{\mathrm{d}t} = \mu_2 E d\cos\theta, \\ \frac{\mathrm{d}\theta(t)}{\mathrm{d}t} = \omega + \mu_3\frac{\mathrm{d}\omega}{\mathrm{d}t}. \end{cases} \quad (2)$$

Since the variation of E is relatively small with comparison to the variation of d, the major dynamics of $\omega(t)$ is from d and the effect of E can then be combined with the proper selection of μ_2. As a result, the enhanced PLL can be constructed as shown in Figure 2.

Comparing the enhanced PLL shown in Figure 2 to the basic PLL shown in Figure 1(b), it can be seen that the enhanced PLL contains a voltage channel to estimate the amplitude of the input signal, in addition to the frequency channel that is very similar to the basic PLL.

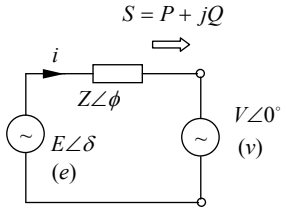
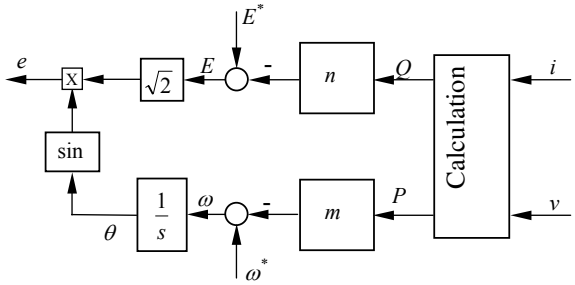


Figure 3. Power delivered to a voltage source through an impedance

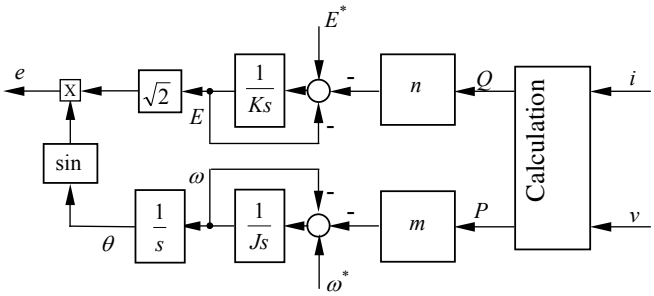
III. Brief Review of Droop Control

Figure 3 illustrates a voltage source $e = \sqrt{2}E\sin\theta$ with $\theta = \omega t + \delta$ delivering power to another voltage source (terminal) $v = \sqrt{2}V\sin\omega t$ through an impedance $Z\angle\phi$. The voltage source could be a conventional synchronous generator or a voltage-controlled inverter. Since the current flowing through the impedance is

$$\begin{aligned}\bar{I} &= \frac{E\angle\delta - V\angle 0^\circ}{Z\angle\phi} \\ &= \frac{E\cos\delta - V + jE\sin\delta}{Z\angle\phi},\end{aligned}$$



(a) without considering the integral effect



(b) with the hidden integral effect explicitly considered

Figure 4. Conventional droop control scheme (for inductive impedance)

the real power and reactive power delivered by the source to the terminal via the impedance can be obtained as

$$P = (\frac{EV}{Z}\cos\delta - \frac{V^2}{Z})\cos\phi + \frac{EV}{Z}\sin\delta\sin\phi,$$
$$Q = (\frac{EV}{Z}\cos\delta - \frac{V^2}{Z})\sin\phi - \frac{EV}{Z}\sin\delta\cos\phi,$$

where δ is the phase difference between the supply and the terminal, often called the power angle. This is the basis of the droop control [16], [17], [18], [19], [20], that is widely adopted in power systems and recently in parallel-operated inverters.

When the impedance is inductive, $\phi = 90°$. Then

$$P = \frac{EV}{Z}\sin\delta \quad \text{and} \quad Q = \frac{EV}{Z}\cos\delta - \frac{V^2}{Z}.$$

When δ is small,

$$P \approx \frac{EV}{Z}\delta \quad \text{and} \quad Q \approx \frac{V}{Z}E - \frac{V^2}{Z},$$

and, roughly,

$$P \sim \delta \quad \text{and} \quad Q \sim E.$$

As a result, the conventional droop control strategy for an inductive Z takes the form

$$E = E^* - nQ,$$
$$\omega = \omega^* - mP,$$

where E^* is the rated RMS system voltage. This strategy, as shown in Figure 4(a), consists of the $Q-E$ and $P-\omega$ droop, i.e., the voltage E is regulated by controlling the reactive power Q and the frequency f is regulated by controlling the real power P. The droop coefficients n and m are selected to meet the desired ratio of the change of voltage, and frequency respectively, to the change of reactive power and real power [1], [21].

The droop control strategy takes different forms when the impedance is of different types; see e.g. [1] for more details. The conventional droop control strategy has some fundamental limitations and is not able to maintain accurate sharing of both real power and reactive power when there are component mismatches, parameter shifts, numerical error, disturbances and noise etc. A robust droop controller is proposed in [21] to overcome these issues. However, these do not affect what is discussed in this paper so the analysis will be based on the conventional droop control strategy.

IV. The Link between Droop Control and Phase-Locked Loops

A. When the Impedance is Inductive

One insightful observation about droop control mentioned in [21] is that the voltage droop control actually includes an integrator because E can be obtained via dynamically integrating[1]

$$\Delta E \triangleq E^* - E - nQ$$

until $\Delta E = 0$ instead of setting $E = E^* - nQ$ statically. This is also true for the frequency droop control, where the frequency ω can be obtained via integrating

$$\Delta\omega \triangleq \omega^* - \omega - mP$$

until $\Delta\omega = 0$. The droop control strategy with the hidden integral effect explicitly considered is shown in Figure 4(b),

[1]Note that this is slightly different from what is done in [21].

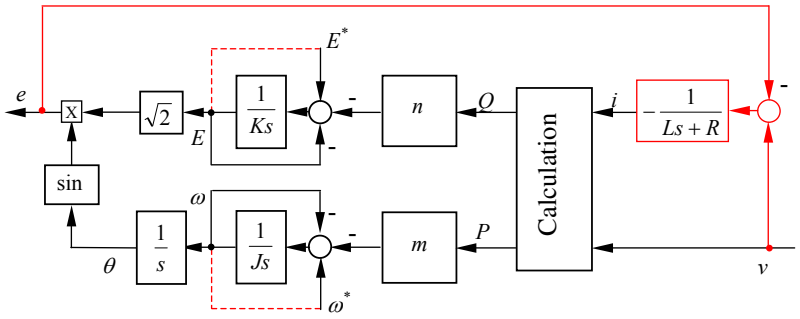


Figure 5. The droop controller with the (inductive) impedance taken into account

where the integral time constants are chosen as J and K for the frequency and voltage channels, respectively. This is equivalent to adding a low-pass filter $\frac{1}{Js+1}$ to the frequency channel and a low-pass filter $\frac{1}{Ks+1}$ to the voltage channel shown in Figure 4(a), respectively. In the steady state, the inputs to the integrators are zero, which recovers the droop control strategy. Apparently, Figure 4(b) becomes Figure 4(a) when the integral time constants are chosen as $K = 0$ and $J = 0$.

The current i flowing through the impedance is

$$i = -\frac{v - e}{Ls + R},$$

where the impedance Z is an inductor with inductance L and its equivalent series resistance (ESR) R. This closes the loop between v and e, as shown in Figure 5. Note that $i = 0$ when $e = v$ and, in this case, the voltage e accurately recovers or estimates the voltage v.

Normally, the real power P and reactive power Q are calculated via measuring the terminal voltage v and the current i. Actually, it is better to use the voltage e than the terminal voltage v for this purpose because e is available internally. The physical meaning of this is to droop the voltage and frequency according to the real power and the reactive power generated by the voltage source e. To some extent, this is more reasonable than using the terminal voltage v because it reflects the genuine real power and reactive power delivered by the voltage source e. In this case, the real power is

$$P = \frac{1}{T}\int_{t-T}^{t} e \times i \, \mathrm{d}t,$$

where T is the period of the system. This is equivalent to passing the instantaneous real power $e \times i$ through the hold filter

$$H(s) = \frac{1 - e^{-Ts}}{Ts}$$

to obtain the (averaged) real power P. The reactive power can be obtained similarly. Define the voltage

$$e_q = \sqrt{2}E\sin(\theta - \frac{\pi}{2}) = -\sqrt{2}E\cos\theta,$$

which has the same amplitude as e but with a phase angle delayed by $\frac{\pi}{2}$ rad. Then, the reactive power can be calculated as

$$Q = \frac{1}{T}\int_{t-T}^{t} e_q \times i \, \mathrm{d}t.$$

For example, for the current $i = \sqrt{2}I\sin\theta_i$, there is

$$Q = \frac{1}{T}\int_{t-T}^{t} 2EI\sin(\theta - \frac{\pi}{2})\sin\theta_i \mathrm{d}t = EI\sin(\theta - \theta_i),$$

which is indeed the reactive power generated by $e = \sqrt{2}E\sin(\theta)$ and i.

The voltage set-point E^* and the frequency set-point ω^* in a droop controller can be set as the rated system values when it is operated in the droop mode, whether it is connected to the grid or it is operated in the standalone mode. They can also be set as the grid voltage and the grid frequency for grid-connected applications to send the desired real power P_{set} and reactive power Q_{set} to the grid (this is not shown in Figure 5 but can be easily implemented by changing $-P$ to $P_{set} - P$ and $-Q$ to $Q_{set} - Q$). If E^* is set as E and ω^* is set as ω, as shown in Figure 5 by the dashed lines, then the voltage e is the same as v in the steady state. This effectively cancels the loop around the integrators $\frac{1}{Js}$ and $\frac{1}{Ks}$. The block diagram shown in Figure 5 can be redrawn, as shown in Figure 6(a), after connecting the dashed lines and calculating the power by using e, as described above. The gains are lumped as $K_e = \frac{n}{K}$ and $K_f = \frac{m}{J}$. This is similar to the widely-used enhanced PLL [12], [11] or the sinusoid-tracking algorithm [13], [22] (which are essentially the same) shown in Figure 2 apart from three major differences: 1) the sin and cos functions are swapped; 2) there is a low-pass filter $\frac{1}{Ls+R}$, or an integrator when $R = 0$; 3) there is a negative sign in the amplitude channel of Figure 6(a). The hold filter $H(s)$ is to filter out the ripples and could/should be inserted into the EPLL/STA to improve the performance so it does not cause any major difference.

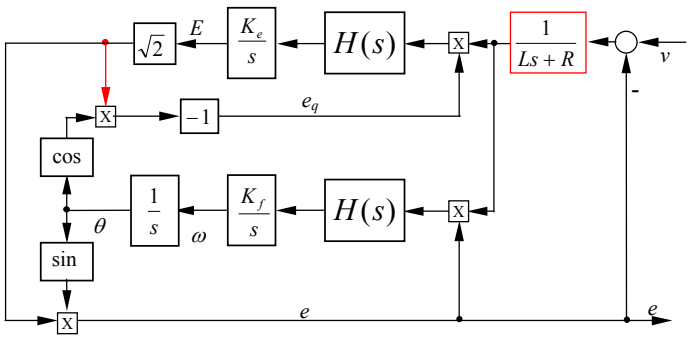
B. When the Impedance is Resistive

When the impedance Z is resistive, $\phi = 0°$. Then

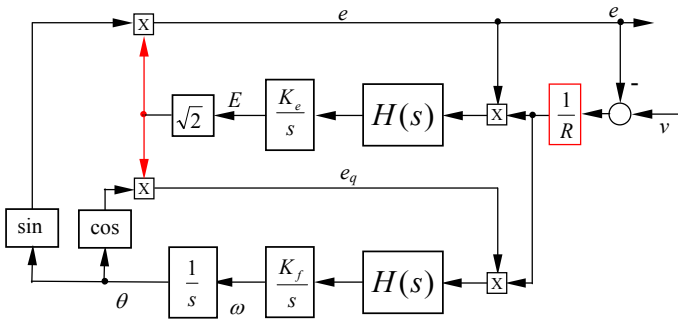
$$P = \frac{EV}{Z}\cos\delta - \frac{V^2}{Z} \quad \text{and} \quad Q = -\frac{EV}{Z}\sin\delta.$$

When δ is small,

$$P \approx \frac{EV}{Z}\delta - \frac{V^2}{Z} \quad \text{and} \quad Q \approx -\frac{EV}{Z}\delta,$$



(a) when the impedance is inductive



(b) when the impedance is resistive

Figure 6. Droop control strategies in the form of a phase-locked loop

and, roughly,

$$P \sim E \quad \text{and} \quad Q \sim -\delta.$$

As a result, the conventional droop control strategy for resistive impedance takes the form

$$E = E^* - nP,$$
$$\omega = \omega^* + mQ.$$

The difference from the inductive case is that the positions of P and Q are swapped and the sign before Q is changed to positive.

Following the arguments in the previous section, this droop controller can be described in the form of a phase-locked loop as shown in Figure 6(b). Comparing it to the enhanced PLL or the STA shown in Figure 2, they are more or less the same, without any major difference. As explained before, the hold filter $H(s)$ is to filter out the ripples and could/should be included in the STA or EPLL to improve the performance so it does not cause any major difference. If the parameters are selected as $R = E$, $\mu_1 = K_e$, $\mu_2 = K_f$ and $\mu_3 = 0$, and the hold filter $H(s)$ is removed, then the two diagrams are exactly the same. This means the droop controller is intrinsically an enhanced phase-locked loop.

There are two channels, a frequency channel and a voltage channel, in both Figure 6(b) and Figure 2. When the voltage channels are ignored, what is left in Figure 6(b) is the frequency droop control and what is left in Figure 2 is a basic PLL. This means the frequency droop control is intrinsically a basic phase-locked loop. This reinforces the conclusion.

V. Conclusions and Discussions

It has been shown in this paper that a droop controller is intrinsically an enhanced phase-locked loop. This bridges the gap between the droop control community and the PLL community and offers fundamental understanding about the operation of power systems, in particular, when there are a lot of renewable energy sources connected via inverters that are equipped with droop controllers. Because of this, there is no longer a need to add a synchronisation unit outside of the droop controller to provide the grid information for synchronisation. This paves the way for developing inverter controllers without a dedicated synchronisation unit to provide the grid information.

There are two ways to apply the findings presented in this paper. One is to apply what is shown in Figure 6 as improved phase-locked loops to provide the frequency, phase and amplitude of the input signal. Another way is to apply the droop control strategy to implement self-synchronised inverters without the aid of a dedicated synchronisation unit. The only change needed is to add a switch into the strategy shown in Figure 5 so that the current i takes the output of the block $\frac{1}{sL+R}$ when the inverter circuit breaker is not turned on and the current i takes the measured current flowing through the inductor when the inverter circuit breaker is turned on.

What is discovered in this paper opens up several lines for future research:

1) The PLLs can be improved by adopting what is done to the droop control strategy. For example, hold filters can be added into the voltage and frequency channels so that the

ripples in the frequency, the amplitude and the phase can be reduced. This also reduces the harmonics in the recovered signal e. A gain $\frac{1}{R}$ or a low-pass filter $\frac{1}{Ls+R}$ can be inserted to speed up the convergence speed. If a low-pass filter $\frac{1}{Ls+R}$ is inserted, then the capability of filtering out the harmonics can be enhanced as well. Because there are different types of droop control strategies for different types of impedance, there are also different types of PLLs. This is why some PLLs adopt a cosine function to detect the phase but some PLLs adopt a sine function to detect the phase. When the impedance is resistive, the corresponding PLL adopts a cosine function to detect the phase; when the impedance is inductive, the corresponding PLL adopts a sine function. The PLLs corresponding to the cases with resistive and inductive impedances are developed in this paper and the PLL corresponding to the case with a capacitive impedance can be developed with ease.

2) The droop control strategies can be improved via looking at the vast literature about PLLs. For example, it is known that the droop control leads to slow response but a PLL can normally lock with the input signal within two cycles, which is much faster than the droop control.

3) It is a challenge to analyse the stability of systems with more than one droop controllers. What is done in the PLL community about the stability of PLLs can be borrowed.

4) Although there are more than 700 papers about droop control found from ieeexplore.ieee.org, the droop control strategy has not been changed fundamentally. Most of them still adopt the conventional droop controller, which is static. The idea presented in this paper to recover the integral effect hidden in the voltage and frequency channels paves a solid foundation for the design of a dynamic droop controller to replace the integrator so that the performance of droop control can be significantly improved. This provides the possibility for the control community to come up with fast and advanced droop control strategies that meet other specifications.

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