

## High current density tunnel diodes for multi-junction photovoltaic devices on InP substrates

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InAlGaAs tunnel diodes, lattice-matched to InP and grown by molecular beam epitaxy, are demonstrated with peak tunnelling current densities exceeding 1200 A/cm<sup>2</sup>. This was achieved by a 20°C reduction in growth temperature for the p-type tunnel diode layers resulting in up to two orders of magnitude improvement in the peak tunneling current density. Secondary ion mass spectrometry measurements reveal that the lower growth temperature reduces unwanted segregation of p-type Be dopants, improving dopant incorporation within the active tunnel diode layers. The diodes are transparent to wavelengths above 1000 nm and are compatible with the bottom junctions of InP-based multi-junction solar cells and with InP-based photonic power converters operating in the telecommunications O- and C-bands. When incorporated into a dual-junction photonic power converter test structure, measurements under 1319-nm laser illumination demonstrate integrated tunnel diode operation, enabling a halving of the short-circuit current and doubling of the open-circuit voltage as compared to a single junction reference device.

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Multi-junction (MJ) photovoltaic (PV) devices offer many advantages over single-junction designs, from record-setting efficiencies in MJ solar cells (MJSCs)<sup>1,2</sup> to high output voltages in MJ photonic power converters (PPCs)<sup>3</sup> that convert monochromatic light from a laser or an LED to electricity (also called optical or laser power converters). MJ PV devices vertically stack multiple epitaxial layers of absorbing series-connected pn junctions which require interconnection via transparent tunnel diodes (TDs). These TDs must provide high peak tunneling current and low differential resistance without introducing parasitic absorption or impeding current flow between adjacent junctions.

The open-circuit voltage of a PV device is related to the bandgap of the absorbing material. In a MJ device, the total voltage is the sum of the voltages of each absorbing junction. For a typical MJSC, each junction is made from a different material that absorbs a different portion of the solar spectrum<sup>2,4</sup>. In contrast, the absorbing junctions of a MJ PPC are all made from the same material<sup>3,5</sup>. The PPC operating voltage scales linearly with the number of junctions while the current drops proportionally. Given the series-connection of the MJ design, the same current flows through each junction. To prevent any one junction from limiting current flow through the entire MJ structure, the thickness of each junction can be optimized to absorb an equal number of photons. PPC junctions are grown optically thin to partition monochromatic illumination.

Under concentrated solar illumination or high intensity input from a laser or LED, irradiance of 100 W/cm<sup>2</sup> generates current densities in the tens of A/cm<sup>2</sup> range in both MJSCs and PPCs<sup>2,6-8</sup>. To operate at such high current densities, TDs must have peak tunneling current densities ( $J_{pk}$ ) that are even higher to avoid limitation of the current flow and minimize resistive power losses and reduced voltage output. TDs with  $J_{pk}$  on the order of 1000 A/cm<sup>2</sup> are routinely used in PV devices based on Ge and GaAs substrates<sup>6,8,9</sup>. TD designs for emerging MJ photovoltaics based on InP substrates are still under development, with an emphasis on arsenide and antimonide semiconductor alloys in the tunneling layers<sup>10-16</sup>.

MJSCs based on InP substrates show great promise as a high efficiency alternative to GaAs-based devices due to the availability of lattice-matched materials with ideal bandgaps for a triple-junction structure<sup>2,10,17-19</sup>. Several TD designs have been proposed by Lumb et al. for this structure<sup>10-13</sup>. TDs designed to link the bottom two junctions (bandgaps of 1.18 eV and 0.74 eV respectively) have been demonstrated with  $J_{pk}$  exceeding 100 A/cm<sup>2</sup>. They are also compatible with MJ PPCs based on InP substrates designed for operation in the

telecommunications O- and C-bands (near 1310 nm and 1550 nm respectively)<sup>20–23</sup>.

In this work, we investigate the effect of growth temperature during molecular beam epitaxy (MBE) on the performance of an InAlGaAs TD grown on InP. We demonstrate a 10- to 100-fold improvement in  $J_{pk}$  resulting from a 20°C reduction in growth temperature, achieving current densities in excess of 1200 A/cm<sup>2</sup>. We also present a dual-junction PPC designed for operation in the telecommunications O-band, showing that the TD can survive the growth of subsequent junctions.

The TDs developed in our experimental work are composed of InAlGaAs lattice-matched to InP, grown by MBE using a Veeco Gen10 system on quarter InP 3"-wafers. An indium-free mounting technique was used. The TDs are designed for full transparency at wavelengths exceeding 1000 nm and for integration between the lower junctions of InP-based MJSCs<sup>2,10,11</sup> or into InP-based PPCs operating in the telecommunications O-band or C-band (demonstrated in this work). The design, shown in Fig. 1a and adapted from work by Lumb et al.<sup>10,12</sup>, uses a p<sup>++</sup>/n<sup>++</sup> junction architecture that enables vertical interconnection of multiple n/p absorbing junctions on a p-type InP substrate. Lattice-matched InAlAs cladding layers on both sides of the TD improve carrier confinement and reduce unwanted dopant diffusion<sup>10</sup>. The TD test structures were grown on n-type InP wafers to maintain the layer growth order in the absence of the absorbing n/p junctions.

The TD structures were grown at different MBE temperatures. For the first device, referred to as HT for “high temperature”, the substrate heater was fixed at 510°C throughout the growth corresponding to an estimated substrate temperature between 465°C and 480°C, as measured by pyrometer and band edge thermometry systems, respectively. For the second device, referred to as LT for “low temperature”, the substrate heater was initially set to 510°C for the entire n-type region. Before starting growth of the first p-type layer, the substrate heater was ramped down to 490°C and then held constant for the entire p-type region. This corresponded to an estimated substrate temperature between 445°C and 460°C, which was an equivalent 20°C reduction in substrate temperature for the p-type epi-layers in sample LT compared to HT.

Epitaxial wafers were processed with a blanket Ni/Ge/Au contact to the n-InP substrate back surface. On the front p-InGaAs cap, lithography and wet chemical etching were used to fabricate square mesas with Pd/Ti/Pd/Au contact pads set back 25 μm from the mesa edge. Fig. 1b shows the metallized TD samples and their positions on the quarter 3"-wafer

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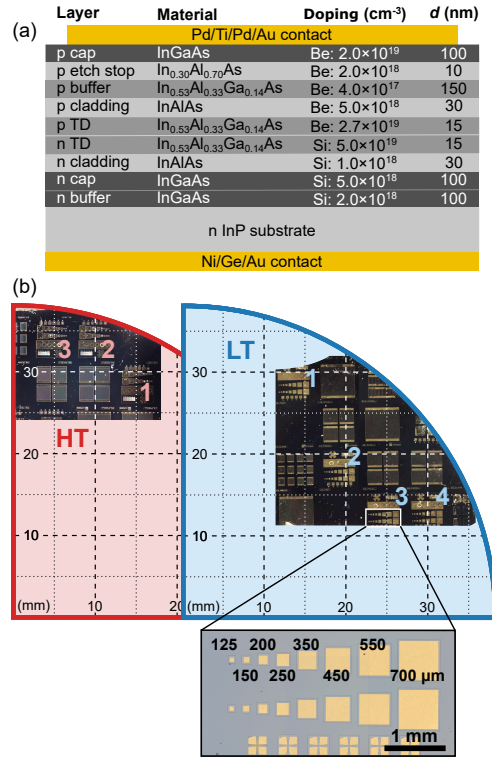


FIG. 1. (a) TD target structure schematics ( $d$  represents the layer thickness). InGaAs and InAlAs layers, except for the etch stop, are lattice-matched to InP. (b) Top view microscope images of tunnel diode samples HT and LT respectively. Relative positions on InP quarter 3"-wafers are shown. The magnified image shows the square diode test pads used for measurements. Side lengths for each diode are given in microns. Note: The orientation of the test pads is upside-down for HT compared to LT.

on which they were processed. The side lengths of the square mesas shown in the inset of Fig. 1b range from 125 to 700  $\mu\text{m}$ . Current-voltage ( $J$ - $V$ ) characteristics were measured using the four-point probe method, with the sample held in place by vacuum on a gold-plated copper chuck. The top contact pads were probed directly while current at the rear side was conducted through the chuck.

Measured  $J$ - $V$  characteristics are shown for several of the TDs in Fig. 2. The operational

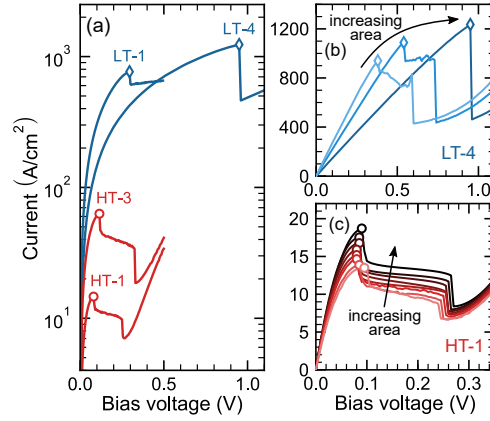


FIG. 2. (a) TD  $J$ - $V$  curves are compared on a semi-logarithmic scale for diodes with a 200  $\mu$ m side length. The position on the wafer is indicated for each curve. (b), (c)  $J$ - $V$  curves on a linear scale for the LT-4 and HT-1 diodes respectively. All diodes shown are from the bottom row. Diodes with side lengths of up to 200  $\mu$ m are shown for LT-4 in (b) and all sizes are shown for HT-1 in (c). See Fig. 1b for diode locations. A marker indicates  $J_{pk}$  in all sub-figures.

region of a typical TD  $J$ - $V$  curve is characterized by a quasi-linear relationship between the tunneling current density and voltage passing through the origin, exhibiting a small differential resistance ( $R_0$ ). At higher voltage, the current density reaches a maximum known as the peak tunneling current density ( $J_{pk}$ ) which limits the highest practical operational intensity. Beyond the peak, the curve enters the negative resistance region where the current density decreases with increasing bias voltage creating a valley before the thermal diffusion current, responsible for conventional diode behaviour, dominates and the current density again increases with bias voltage. The negative resistance region of the graph is typically unresolved in time-averaged experimental measurements such as those in Fig. 2.

Fig. 2a shows the  $J$ - $V$  characteristics for TDs with a side length of 200  $\mu$ m on a semi-logarithmic scale. Two curves are shown for each nominal growth temperature, corresponding to  $J$ - $V$  measurements performed at different positions on their respective quarter wafers, to show the range of performance for each sample. LT significantly outperforms HT, with  $J_{pk}$  1-2 orders of magnitude larger.

Fig. 2b and c show the  $J$ - $V$  characteristics on a linear scale for the LT-4 and HT-1 diodes.

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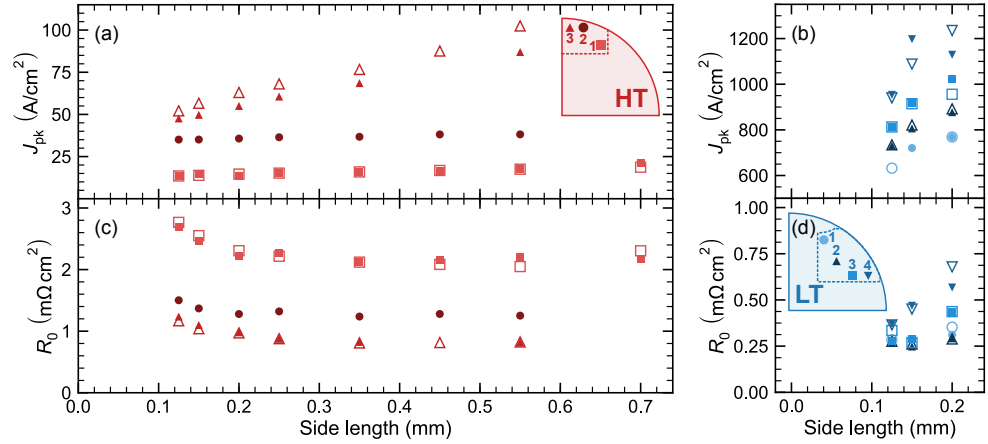


FIG. 3. (a), (b)  $J_{pk}$  as a function of diode side length for HT and LT respectively. (c), (d) differential resistance  $R_0$  as a function of diode side length for HT and LT respectively. The diode positions on each wafer are indicated. Solid symbols correspond to the top row of diodes and open symbols to the bottom row (see Fig. 1b)

For diode HT-1,  $J_{pk}$  consistently increases with increasing diode size, suggesting that edge effects such as perimeter recombination may have an impact on the device performance. A similar effect is observed for LT-4, although the peak current density is less well resolved due to series resistance effects that impact the shape of the curve<sup>6,9</sup>. The larger diodes were not measured for sample LT because the high measurement currents exceeded the damage threshold of our fabricated devices.

$J_{pk}$  is shown as a function of diode side length for HT and LT in Fig. 3a and b, respectively. For sample HT, the diodes closest to the wafer edge have higher  $J_{pk}$ , increasing by a factor of 4 from HT-1 to HT-3. Considering the larger  $J_{pk}$  for the lower temperature growth, LT, the positional dependence for sample HT indicates a temperature gradient across the wafer during growth, with lower temperature near the substrate edges resulting in higher tunneling currents. A similar trend is observed for LT, with the notable exception of the LT-1 diodes, which have the lowest  $J_{pk}$  values despite being closer to the wafer edge than LT-2 and LT-3. This implies that the substrate temperature profile may be influenced by multiple factors<sup>24</sup>.

The results in Fig. 3a and b also confirm that  $J_{pk}$  generally increases with diode size. This trend is observed for all of the measured diodes, including HT-1 and HT-2. Mesa edge effects including trap states or fixed charges that counteract tunneling near the perimeter may be impacting the device performance, changing the effective area for current flow through the mesa structure. Another important factor is the spatial variation that results from non-uniform substrate temperature during growth. This positional effect influences the electrical response of diodes along a single row (see Fig. 1b), likely enhancing the observed increase in current density with diode size due to the spatial orientation of the diodes on each wafer in some cases.

$R_0$  is shown as a function of diode side length for both samples in Fig. 3c and d. For sample HT, the resistance ranges from 0.8 to 2.8  $m\Omega\text{ cm}^2$  and is smallest for the diodes closest to the wafer edge, where we expect that the growth temperature is lower.  $R_0$  is a factor of 4 smaller for sample LT, ranging from 0.2 to 0.7  $m\Omega\text{ cm}^2$  for all diode sizes and positions.

The top contact resistivity for sample LT was measured as  $\sim 0.006\text{ m}\Omega\text{ cm}^2$ . For HT, a much larger top contact resistivity of  $\sim 0.36\text{ m}\Omega\text{ cm}^2$  was found. Given the 25  $\mu\text{m}$  gap between the contact pad and the mesa edge, the contribution of the top contact to  $R_0 = J/V$  is proportional to  $L^2/(L - 25\text{ }\mu\text{m})^2$  where  $L$  is the mesa side length. We therefore expect a decrease in  $R_0$  with diode size, as observed in Fig. 3c.  $R_0$  begins to stabilize as the ratio  $L^2/(L - 25\text{ }\mu\text{m})^2 \rightarrow 1$ . The contribution of the top contact to  $R_0$  is clearly observed for sample HT. For sample LT, the top contact resistivity is small enough that its contribution to  $R_0$  is negligible.

High doping concentrations ( $> 10^{19}\text{ cm}^{-3}$ ) in a thin, abrupt junction are essential characteristics of a high-performance tunnel diode, but this is challenging to achieve due to unwanted dopant diffusion and segregation during growth. Precise placement of very high Be doping levels can be particularly challenging to achieve<sup>25</sup>. Therefore, secondary ion mass spectrometry (SIMS) was performed on unprocessed wafers by EAG Laboratories using a Dynamic-SIMS PHI ADEPT-1010 system to measure the Si and Be doping profiles through the active layers of the TDs.

Comparisons between the Si and Be doping profiles for HT and LT measured by SIMS are shown in Fig. 4a. Positions are measured relative to the centre of the TD, with the substrate towards the positive side of the position axis. The target doping profile is indicated

by the shaded region and refers to the desired active dopant concentration, whereas SIMS measures the total dopant atomic concentration, both active and inactive. Si incorporation is consistent between the two samples as the substrate heater temperature was 510°C for both samples in the n-doped region. Be, on the other hand, tends to segregate during growth leading to the dopant distributing through subsequent growth layers rather than fully incorporating in the region where it was deposited. The 20°C lower growth temperature reduces the unwanted Be segregation, thereby improving the Be incorporation in the TD layers of the LT sample. The striking difference in Be segregation for the two samples coupled with the observed variability in tunnelling performance between the two samples and across a single substrate highlight the sensitivity of these Be-containing TDs to the growth temperature.

Fig. 4b applies a linear scale for the doping profiles in the immediate vicinity of the active layers, highlighting the difference in the Be doping concentration within the TD for the two samples. Due to the resolution of the SIMS measurements across the narrow Be peaks, direct comparison of the Be peaks is somewhat uncertain. Per the SIMS measurements, the maximum Be concentrations are  $\sim 5 \times 10^{19}$  and  $\sim 7 \times 10^{19} \text{ cm}^{-3}$  for HT and LT, respectively. Integrating the Be concentration within the central p TD and n TD layers yields integrated Be concentrations of  $\sim 5.0 \times 10^{13}$  and  $\sim 6.7 \times 10^{13} \text{ cm}^{-2}$  for HT and LT respectively. Higher p-type doping will result in a more abrupt junction with a narrower depletion region, increasing  $J_{pk}$ .

To demonstrate the functionality of the LT TDs within a functional device, we compared single- and dual-junction PPCs, the latter of which required one TD to interconnect each absorbing junction. The  $\text{In}_{0.53}\text{Al}_{0.33}\text{Ga}_{0.14}\text{As}$  absorbing layers with a 0.88 eV bandgap were grown by MBE on p-type InP wafers. The PPCs were designed for monochromatic power conversion from a laser source in the telecommunications O-band. The single-junction PPC has an absorber thickness of 4.1  $\mu\text{m}$ , while the dual-junction PPC consists of a 0.76- $\mu\text{m}$  absorber atop a TD and a 4.1- $\mu\text{m}$  absorber (schematic shown in Fig. 5a). For the single-junction PPC, the substrate heater was held at 510°C for the entire growth. For the dual-junction PPC, the heater temperature was ramped down from 510°C to 490°C between the highly doped tunneling layers, as for the LT TDs, and held at the lower temperature for the remainder of the epitaxy.

PPC devices were processed with a blanket Pd/Zn/Pd/Au contact to p-InP on the rear



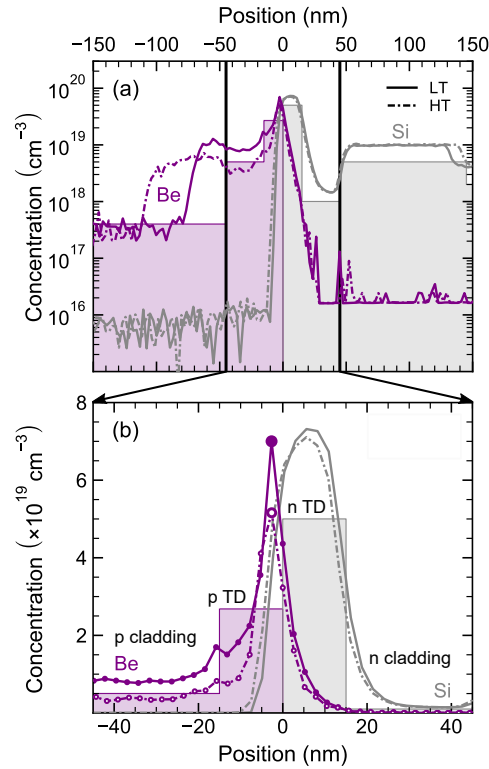


FIG. 4. SIMS measurements of Be and Si concentrations in HT and LT. Position zero aligns with the centre of the tunnel diode. Doping concentrations are shown on a logarithmic scale across a 300 nm range surrounding the TD in (a), where the active TD and InAlAs cladding region is bounded by the solid black lines. In (b), the central TD region is shown with concentrations on a linear scale. Target doping concentrations are indicated by the shaded regions. Peak Be concentrations are indicated by the large markers in (b).

face, followed by rapid thermal annealing at 400°C for 2 minutes to achieve ohmic behaviour. Pd/Ti/Pd/Au contacts were patterned on the top face and wet chemical etching was used to define mesas with dimensions of 1.65 mm × 1.85 mm. Two 200-μm wide busbars are connected by 6-μm wide gridlines on a 114-μm pitch, resulting in a shading factor of 5%. The metallization is set back by 25 μm from the mesa edge. The n-type InGaAs cap was removed between the contacts using a wet chemical etch.

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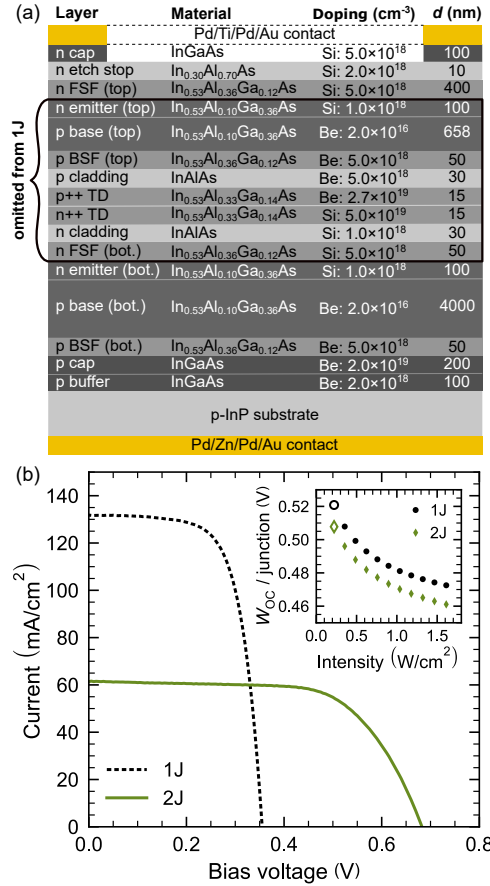


FIG. 5. (a) PPC target structure schematic ( $d$  represents the layer thickness). InGaAs and InAlAs layers, except for the etch stop, are lattice-matched to InP. (b) 1- and 2-junction InAlGaAs operating  $J$ - $V$  characteristics under 1319 nm laser illumination at an intensity of  $0.22 \text{ W/cm}^2$ . The inset shows the average  $W_{OC}$  per junction as a function of illumination intensity, up to  $1.6 \text{ W/cm}^2$ . The open symbols correspond to the  $J$ - $V$  curves shown.

PPC  $J$ - $V$  characteristics were measured under 1319-nm illumination from a Dilas conduction-cooled single bar fiber-coupled laser. Two probes were used to conduct current from the top busbars with the rear-side current being conducted through a gold-plated copper chuck maintained at  $25^\circ\text{C}$  using a thermoelectric cooler. The  $J$ - $V$  characteristics

are shown in Fig. 5b for both devices measured under monochromatic 1319 nm illumination with an intensity of  $0.22 \text{ W/cm}^2$ , averaged over the  $0.0305 \text{ cm}^2$  mesa area. As expected, the dual-junction  $V_{OC}$  is nearly double the single-junction  $V_{OC}$  due to the integrated series-connection of two junctions, each producing similar voltage. The single-junction device was designed to absorb 95% of the incident light. When current-matched, a dual-junction device should produce close to half the short-circuit current density of the single-junction at the laser wavelength<sup>20</sup>.

Due to a slightly In-rich quaternary composition in the dual-junction device, its bandgap energy was red-shifted by  $\sim 30 \text{ meV}$  compared to the perfectly lattice-matched single-junction structure. Therefore, rather than a direct comparison of the  $V_{OC}$ , we can instead compare the bandgap-voltage offset,  $W_{OC} = (E_g/q) - V_{OC}$ , where the bandgap energies ( $E_g$ ) are 0.88 eV and 0.85 eV for the single- and dual-junction PPCs, respectively. The average  $W_{OC}$  per junction is shown as a function of illumination intensity up to  $1.6 \text{ W/cm}^2$  in the Fig. 5b inset. The  $W_{OC}$  values are similar for both devices across the intensity range indicating that the TD is providing an effective series connection between the junctions with minimal voltage loss. The  $W_{OC}/\text{junction}$  is slightly lower for the dual-junction device because the thinner top junction is expected to have a larger  $V_{OC}$  compared to the thick bottom junction and the single-junction PPC, as discussed in Ref. 20, due to its higher photo-generated carrier concentration.

In summary, we have developed an InP-based TD composed of lattice-matched InAlGaAs that is transparent for wavelengths  $>1000 \text{ nm}$ . The peak tunneling current density  $>1200 \text{ A/cm}^2$  makes it suitable for MJ device operation at illumination intensities up to and exceeding  $100 \text{ W/cm}^2$ . We show a one to two order of magnitude improvement in the peak tunneling current density following a  $20^\circ\text{C}$  reduction in nominal growth temperature during Be incorporation due to reduced Be segregation. The results demonstrate that this TD design is viable for use and is a worthwhile platform for further study. Finally, we demonstrate the functionality of the TD embedded in a dual-junction PPC, generating the expected doubling of  $V_{OC}$  compared to a single-junction reference device. The sensitivity of the Be-containing tunnel diodes to growth temperature that we observe in this work highlights the importance of keeping tight tolerances for temperature-uniformity across the wafer during growth to achieve device reproducibility.

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## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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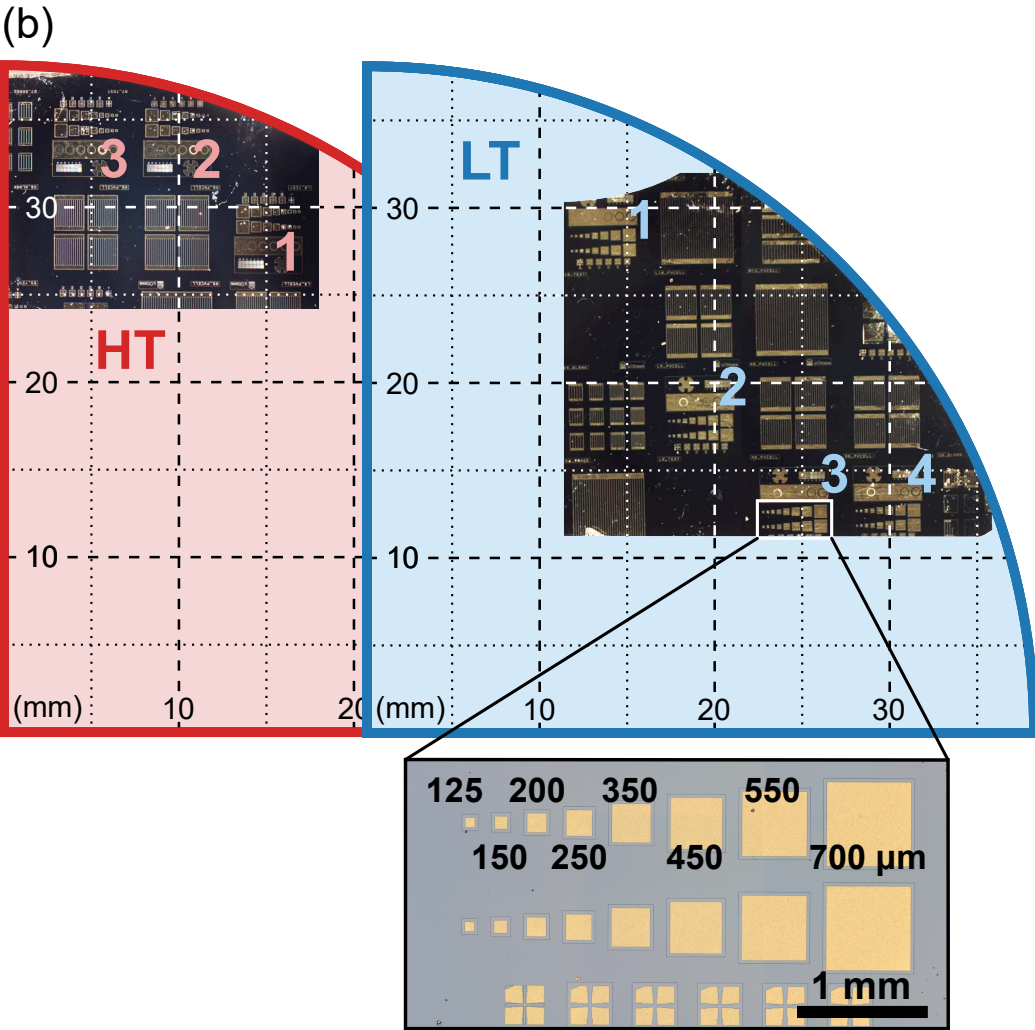
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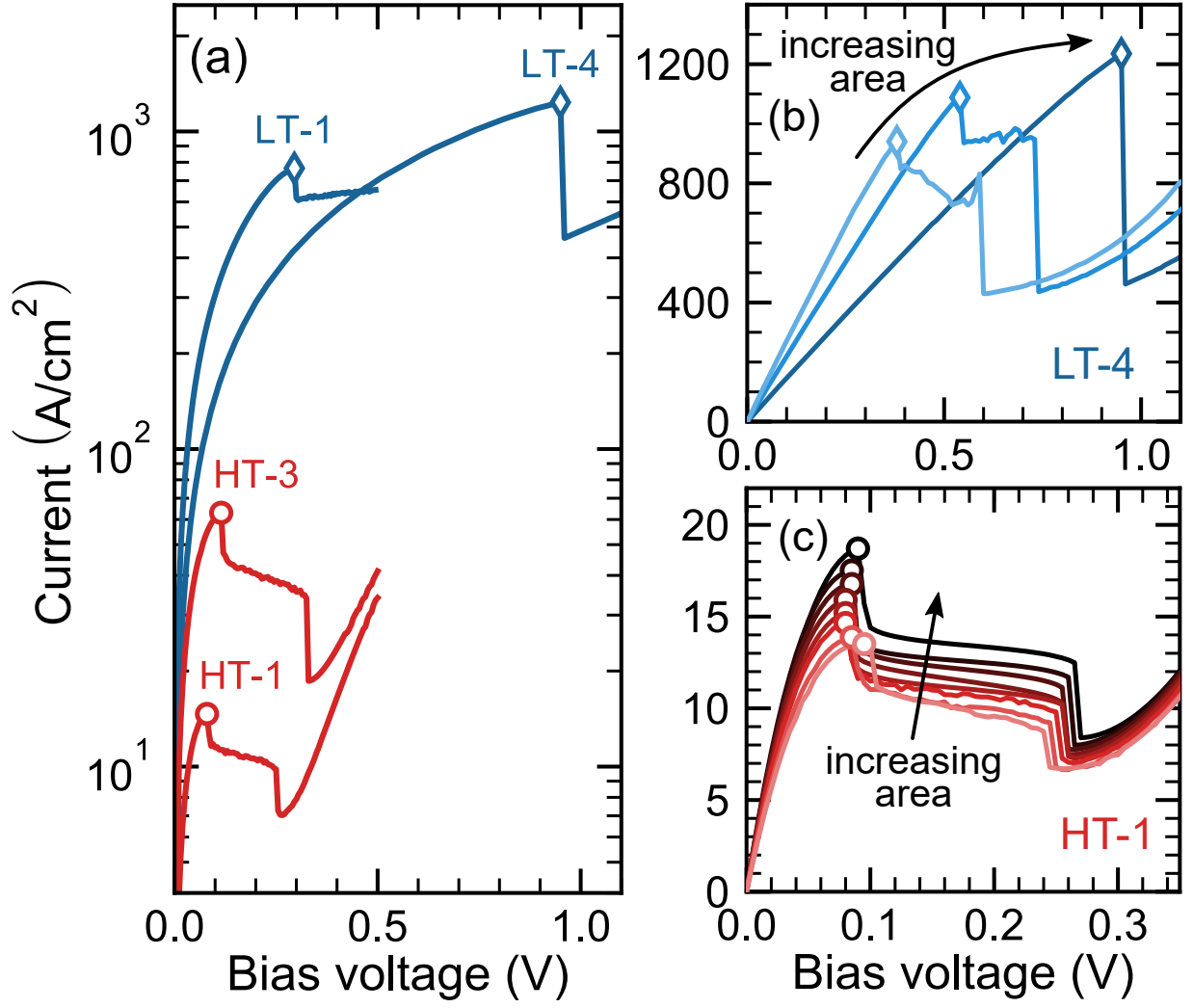
(a)

Layer	Material	Doping (cm <sup>-3</sup> )	d (nm)
Pd/Ti/Pd/Au contact			
p cap	InGaAs	Be: 2.0×10 <sup>19</sup>	100
p etch stop	In <sub>0.30</sub> Al <sub>0.70</sub> As	Be: 2.0×10 <sup>18</sup>	10
p buffer	In <sub>0.53</sub> Al <sub>0.33</sub> Ga <sub>0.14</sub> As	Be: 4.0×10 <sup>17</sup>	150
p cladding	InAlAs	Be: 5.0×10 <sup>18</sup>	30
p TD	In <sub>0.53</sub> Al <sub>0.33</sub> Ga <sub>0.14</sub> As	Be: 2.7×10 <sup>19</sup>	15
n TD	In <sub>0.53</sub> Al <sub>0.33</sub> Ga <sub>0.14</sub> As	Si: 5.0×10 <sup>19</sup>	15
n cladding	InAlAs	Si: 1.0×10 <sup>18</sup>	30
n cap	InGaAs	Si: 5.0×10 <sup>18</sup>	100
n buffer	InGaAs	Si: 2.0×10 <sup>18</sup>	100
n InP substrate			
Ni/Ge/Au contact			



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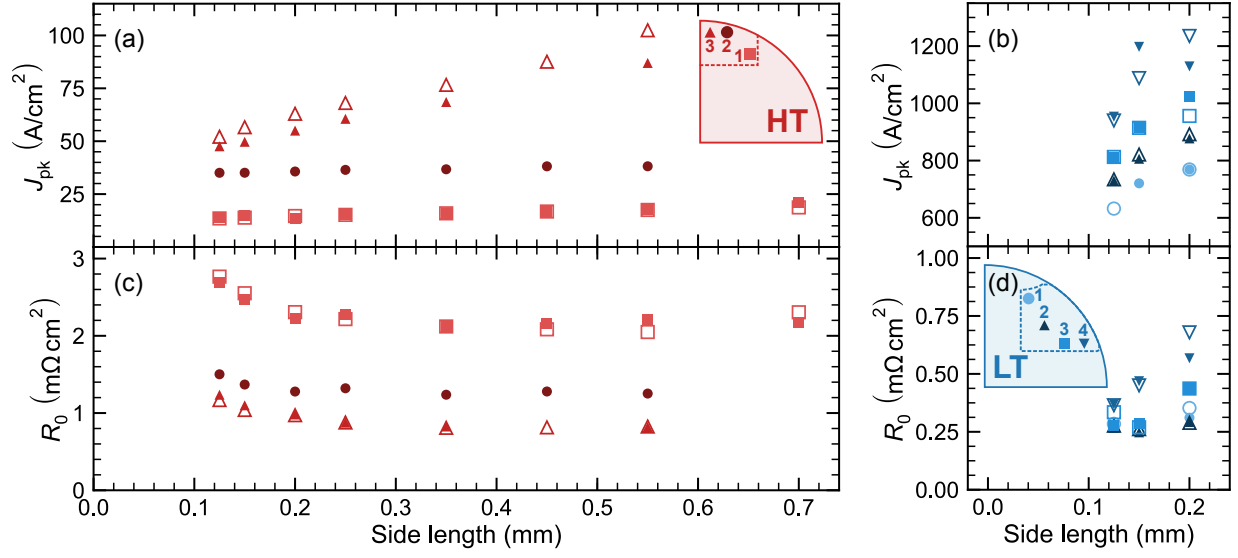
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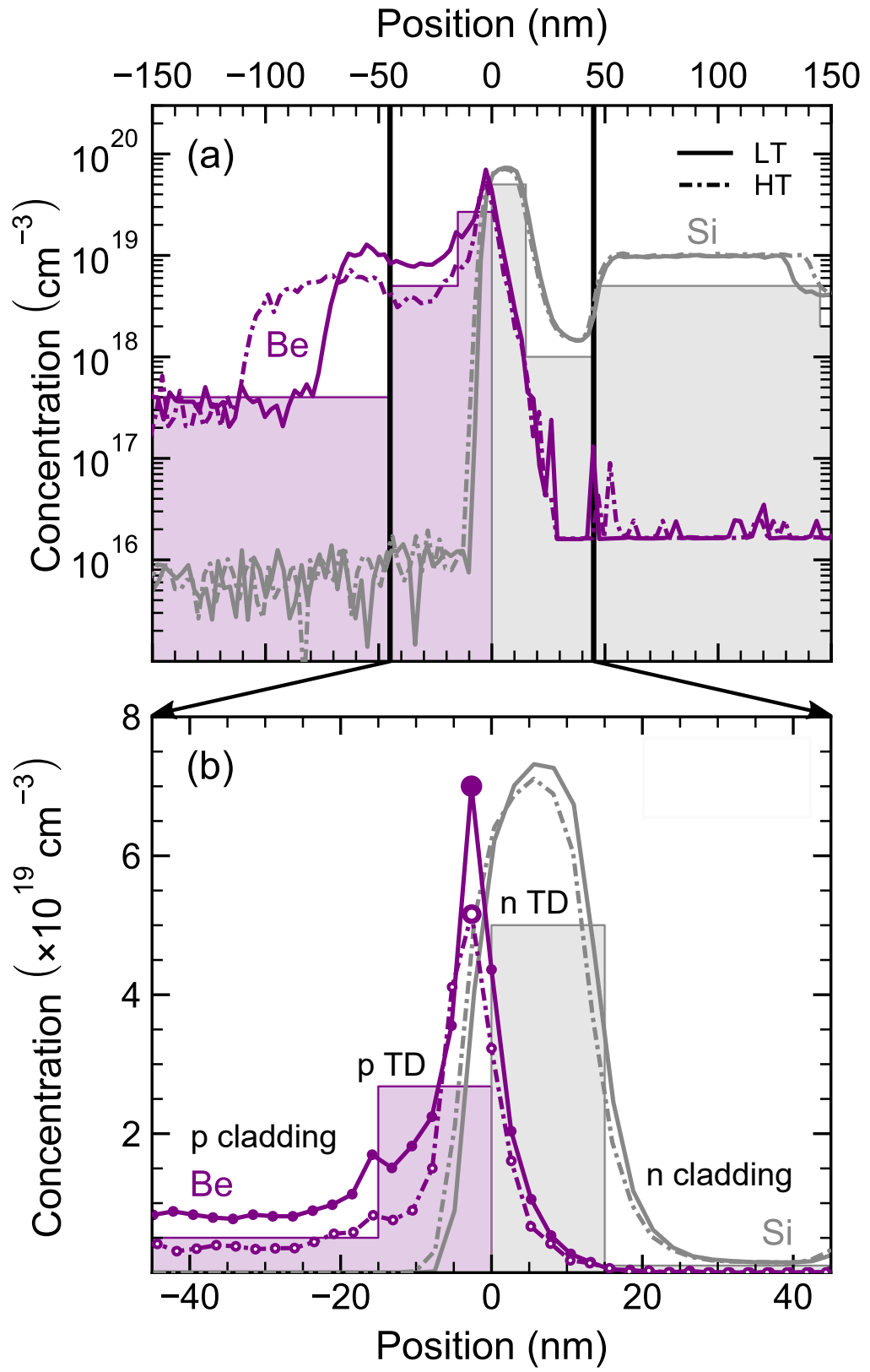
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